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Docket: 0057-2362-2YY

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

Re: Group Art Unit: 2811
Serial No.: 09/176,315
Filed: OCTOBER 22, 1998
Applicant: SHIGENOBU MAEDA, ET AL.
For: METHOD OF DESIGNING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE RECORDING MEDIUM

Attached hereto for filing are the following papers:

APPEAL BRIEF WITH APPENDIX (in triplicate)
PETITION FOR EXTENSION OF TIME (1 MONTH)

Our check in the amount of **$ 430.00** is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R. 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate of this sheet is enclosed.

Respectfully submitted,

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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

SHIGENOBU MAEDA ET AL. : EXAMINER: CRANE, S.

SERIAL NO: 09/176,315 :

FILED: OCTOBER 22, 1998 : GROUP ART UNIT: 2811

FOR: METHOD OF DESIGNING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE AND RECORDING MEDIUM

APPEAL BRIEF

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

This is an appeal of the Final Rejected dated June 5, 2001, of Claims 1-5 and 18 that is hereinafter referred to as FR. A Notice of Appeal was timely filed on November 5, 2001.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Mitsubishi Denki Kabushiki Kaisha having a place of business at 2-3 Marunouchi 2-chome, Chiyoda-ky, Tokyo 100-8310, JAPAN.

II. RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative, and the assignees are aware of no appeals which will directly affect or be directed affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claim 1-5 and 18 stand finally rejected, which forms the basis for this appeal. Claims 6-16 and 19 have been indicated to be allowable if rewritten to be in independent form so that Claim 6 would include all of the limitations of Claims 5, 3 and 1; Claim 9 would include all of the limitations of Claims 5, 3, and 1; Claim 11 would include all of the limitations of Claims 5, 3, and 1; Claim 12 would include all of the limitations of Claim 5, 3, and 1; Claim 16 would include all of the limitations of Claim 5, 3 and 1; and Claim 19 would include all of the limitations of Claims 18, 4, and 2. Claims 17 and 20, the only other claims remaining in this application, have been withdrawn from consideration by the Examiner as being to species that were non-elected with traverse.

IV. STATUS OF THE AMENDMENTS

No amendments were filed after the FR. Instead, a Request for Reconsideration was filed on September 5, 2001, but this request was not considered to overcome the rejections applied to Claims 1-5 and 18 as indicated by the Advisory Action mailed on October 2, 2001. The attached Appendix I reflects the claims as last amended on October 5, 2000.[1]

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[1]This Advisory Action erroneously states that the Amendment filed October 5, 2000 instructed the deletion of the frequency variable character "f" from Claim 1. This amendment contained no such instruction to delete the character "f" which appears at actual line 21 of Claim 1; instead, it instructed the deletion of "(F)" (the indication of the units of capacitance) at actual line 23 of Claim 1, not the character "f"at actual line 21 of Claim 1. Even if the PTO erroneously used the page line numbers at the side of page 43 instead of actually counting line numbers, the PTO should not have deleted the character "f" because "f" and "(F)" are clearly not the same. Moreover, the further instructions to delete "(Ω)" at line 24 of Claim 1 and "(Hz)" at line 27 of Claim 1 should have served to remove any doubt as to how line numbers were being counted with the first line of Claim 1 being line 1, not line 3, and so on.

V. SUMMARY OF THE INVENTION

The present invention is directed to a method of determining a layout pattern for an MOS transistor and the MOS transistor resulting from using this layout pattern. This MOS transistor layout pattern that is used to form an MOS transistor SOI structure like that of FIGS. 1-2, for example, is required to be determined based upon an operating clock frequency that is equal to or greater than 500 MHZ while still providing the MOS transistor SOI structure with stable operation. In order to provide for this highspeed operation that is stable, the layout pattern must be determined to satisfy the conditional expression $R \cdot C \cdot f < 1$, where R represents the resistance of a fixed potential transmission path extending from a body contact on a body portion of the MOS transistor to a body region that is between a first semiconductor region of first conductivity type and a second semiconductor region also of the first conductivity type that are both formed in an SOI layer of the MOS transistor, C represents the gate capacitance of the MOS transistor, and f represents the operating frequency of a predetermined clock that is equal to or greater than 500 MHZ. The flow chart of FIG. 4 summarizes the steps of the method and notes the generation of a layout pattern with a maximum allowable gate width W_{max} that is determined to satisfy this conditional expression. FIG. 5 shows an example of using a layout pattern generating device to implement the method and provide layout pattern data to be used to actually make the MOS transistor.

In another aspect of the invention, an MOS transistor having an SOI structure is formed using a layout pattern for the MOS transistor determined to satisfy the conditional expression $(R \cdot C)/td < 1$. In this conditional expression, td represents signal propagation delay time (s) required for the MOS transistor that is less than 50 ps, with the parameters R and C being those noted above. This is summarized in the flow diagram of FIG. 7, for example,

which notes generation of a layout pattern with the maximum allowable gate width W_{max} that is determined to satisfy this conditional expression.

VI. ISSUE

The only issue is whether or not the subject matter of Claims 1-5 and 18 would have been obvious to one or ordinary skill in the art in the sense of 35 U.S.C. §103 over Iwamatsu et al (the 1995 article entitled "*High-Speed* 0.5 μm *SOI 1/8 Frequency Divider with Body-Fixed Structure for Wide Range of Applications*) (Iwamatsu) in view of Agari (JP 6-224302) and Chen et al (U.S. Patent No. 5,767,549) (Chen).

VII. GROUPING OF THE CLAIMS

Claims 1, 2, 5, and 18 will stand or fall separately and are argued separately below. Claim 3 will stand or fall with Claim 1 and Claim 4 will stand or fall with Claim 2.

VIII. ARGUMENT

1. The subject matter of Claims 1 and 2 has not been properly analyzed.

Turning to the outstanding final rejection of Claims 1 and 2 under 35 U.S.C. §103 as unpatentable over Iwamatsu in view of Agari and Chen, it is first noted that the FR adopts the reasoning presented in the Office Action mailed on December 20, 2000, hereinafter referred to as the December 20 Action. This December 20 Action first incorrectly notes that Iwamatsu "teaches each of the structural elements of Claims 1 and 2" while ignoring that the subject matter of Claims 1 and 2 actually involves methods of designing a semiconductor device including a MOS transistor, where each of these claims require a different manner of

determining a layout pattern for the MOS transistor. The layout pattern of Claim 1 must be determined based on the operating frequency of a predetermined clock that must have a frequency "f" greater than 500 MHZ while the layout pattern of Claim 2 must be determined based on a signal propagation delay time "td" required for the MOS transistor that is less than 50 ps.

Claim 1 further requires the meeting of a specific conditional expression "R•C•f<1," with "f" as defined above, with R being the resistance of a fixed potential transmission path extending from a body contact on a body portion of the MOS transistor to a body region that is between a first semiconductor region of first conductivity type and a second semiconductor region also of the first conductivity type, with the first and second semiconductor regions both being in an SOI layer of the MOS transistor, and C being the gate capacitance of the MOS transistor. Claim 2 further requires the meeting of a specific conditional expression "(R•C)/td<1," with "td," "R," and "C" as defined above.

While Agari may teach designing a semiconductor device in a manner minimizing RC delay from the resistance value and the capacitance value of each wiring part using a wiring layout and Chen may teach controlling doping of the body of an SOI device so that the RC time constant in the body link or recessed region 20 from a respective channel to the substrate contact 39 can be as short as or less than 1 nsec, a wiring layout is not a layout pattern of an MOS transistor and doping is not a step of providing an operating frequency of a predetermined clock, much less a step of determining a layout pattern of an MOS transistor based on the operating frequency of such a provided predetermined clock as Claim 1 recites. Thus, even if the teachings of Agari and Chen are in some reasonable manner combined with Iwamatsu, the result would not be the subject matter of Claim 1.

With further regard to Claim 2, the steps of providing a signal propagation delay time that is less than 50 ps for a MOS transistor and then determining a layout pattern of this MOS transistor based on said signal propagation delay time are also clearly not taught by Agari or Chen. Thus, even if the teachings of Agari and Chen are in some reasonable manner combined with Iwamatsu, the result would not be the subject matter of Claim 2.

Moreover, even as to semiconductor devices of Claims 3 and 4, the criticality of the layout patterns being appropriately determined cannot be dismissed in terms of the structural relationships that still must exist in the manufactured semiconductor device in terms of the above-noted parameters of "R" and "C" having values that taken with a frequency "f" having a value greater than 500 MHZ will satisfy the conditional expression "R•C•f<1" and that taken with a propagation delay time "td" having a value that is less than 50 ps will satisfy the conditional expression "(R•C)/td<1."

Proper and reasonable interpretations of claim limitations are clearly required if the PTO is to perform its well established duty of properly analyzing the differences between the claimed subject matter and the prior art. See In re Dembicziak, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999) as follows:

> A claimed invention is unpatentable if the differences between it and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. §103(a) (Supp. 1998); *See Graham v. John Deere Co.*, 383 U.S. 1, 14, 148 USPQ 459, 465 (1966). The ultimate determination of whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including: (1) The scope and content of the prior art; (2) the level of ordinary skill in the prior art; (3) the differences between the claimed invention and the prior art; and (4) objective evidence of nonobviousness. *See Graham*, 383 U.S. at 17-18, 148 USPQ at 467; *Miles Labs, Inc. v. Shandon, Inc.*, 997 F.2d 870, 877 27 USPQ2d 1123, 1128 (Fed. Cir. 1993).

Further in this regard, note that Dembicziak indicates that "the Graham decision (148 USPQ at 467) requires "strict observance" of factual predicates to any determination of obviousness. Here, however, there has been no attempt to properly analyze the differences between the claimed invention and the prior art by giving reasonable meaning and effect to every limitation in independent Claims 1 and 2.

It is also well established that "every limitation positively recited in a claim must be given effect in order to determine what subject matter that claim defines." In re Wilder, 166 USPQ 545, 548 (CCPA 1970). Note also In re Wilson, 165 USPQ 494, 496 (CCPA 1970) ("all words in a claim must be considered in judging the patentability of that claim against the prior art").

Besides failing to properly analyze the limitations of Claims 1 and 2 and to properly consider all the words of these claims, the FR misinterprets the fair and reasonable teachings of Agari and Chen along with those of Iwamatsu.

2. The teachings of Iwamatsu, Agari, and Chen have not been properly construed.

The FR first correctly noted that Agari teaches designing a semiconductor device in a manner "minimizing RC delay from the resistance value and the capacitance value of each wiring part" (emphasis added, see the bottom of page 2 of the December 20 Action). However, the FR appears to have then ignored that the teachings of Iwamatsu include the illustrated X and Y wiring lines and that if the artisan is to take the teachings of Agari in proper context, as they must be taken, see In re Wasslau, 147 USPQ 391, 393 (CCPA 1965), then all that Agari can be said to reasonably teach is that a wiring lay out having a capacitance "C,"as to spacings between wiring parts that have a particular resistance "R" produce an RC delay, which is the RC delay "from the resistance value and the capacitance

value at each wiring part" (emphasis added) that Agari clearly teaches "minimizing" by a wiring layout design that is clearly not the claimed layout of an MOS transistor on an SOI layer.

Accordingly, what is clearly missing from the rejection is some reasonable basis to expand the teachings of Agari from a concern with wiring spacing capacitances and associated wiring resistance having an RC delay to be minimized into a concern with the capacitance of a gate and the resistance of a fixed potential transmission path extending from at least one body contact to a body region of Iwamatsu, where neither Agari or Iwamatsu present any reason to believe that the artisan would be concerned with wiring delay other than relative to illustrated X and Y wiring lines of Iwamatsu given the above-noted teachings of Agari clearly relate to designing a wiring mask layout for external wiring, not the layout of an MOS transistor formed on an SOI layer. In this regard, the response filed on March 20, 2001, indicated that:

> The Action appears to suggest (at the top of page 3) that Agari somehow teaches minimizes the RC time constant of a body contact because of the improperly extracted reference to a "wiring part" at the bottom of page 2 of the Action. However, it is clear that Agari actually teaches the optimizing of wiring line widths and spacings in terms of minimizing the RC delay of a "wiring part," where the term "wiring" is one the artisan would not use to describe a body contact portion. Thus, when the "PURPOSE" and all of the "CONSTITUTION" portions of the "ABSTRACT" are read together to understand what Agari is referring to as a "wiring part" and the typical use of the term "wiring" is considered, it is clear that line width and spacing are relative to standard surface wiring and this width and spacing of the "wiring part" are controlled to minimize RC delay by controlling values of resistance and capacitance corresponding thereto. In this last regard, it is well established to be "impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art" (In re Wasslau, 147 USPQ 391, 393 (CCPA 1965)).

Thus, the teachings of Agari taken in context, as they must be taken, are clearly stated to be directed determining a wiring mask layout "so that the line and space at each wiring

part may be the optimum line and space calculated respectively" (emphasis added). The FR improperly ignores that it is time delays due to wiring parts that have lines with capacitance inducing spaces there between that are the concern and improperly suggests that these clear teachings of Agari as to planning actual wiring layout with well defined spaces and corresponding capacitance effects would be interpreted as teachings to apply to something other than the similar surface wiring lines shown as x and y by Iwamatsu. Missing, however, is the "logical reason apparent from positive, concrete evidence of record" (In re Regel, 188 USPQ 136, 139 n.5 (CCPA 1975)) why the artisan would have been reasonably led to conclude that something other than planning the layout of wiring like the wiring lines shown as x and y by Iwamatsu was being suggested by Agari.

A. Claims 1 and 3.

Moreover, there are clearly no teachings or suggestions in either Iwamatsu or Agari to design the layout of anything to "satisfy the conditional expression $R \cdot C \cdot f < 1$ where C = the gate capacitance of said MOS transistor, R= the resistance of a fixed potential transmission path extending from said at least one body contact to said body region and f = the operating frequency of said predetermined clock, and $f \geq 500$ MHZ" as required by Claim 1.

Apparently realizing that the mere reference to minimizing "RC delay from the resistance value and the capacitance value at each wiring part" in the determination of "optimum line width and space at every wiring part" (see the "PURPOSE" portion of the Agari abstract) for determining a wiring mask layout teaches nothing as to satisfying the above-noted Claim 1 layout design criteria involving the capacitance of a gate electrode and the resistance of an entirely separate fixed potential transmission path, the December 20 Action relied upon in the FR looked to the Chen teaching at col. 7, lines 29-34 for the

missing logical basis to suggest that the artisan would employ the method of Claim 1 in making the semiconductor device of Iwamatsu.

However, this relied upon teaching of Chen only teaches doping the body of an SOI device so that "the RC time constant in the body link or recessed region 20 from a respective channel to the substrate contact 39 can be as short as or less than 1 nsec." (Emphasis added.) The concern with the values of "R" and "C" in the body link or recessed region 20 could not be more clearly stated. Nevertheless, the examiner would rely only upon the clarity of the exact words appearing in Chen as to the body link or recessed region being addressed, see the last line of page 2 of the December 20 Action relied upon in the FR ("It is clear that the recessed region or body link is addressed, because this is exactly what the sentence says."), while ignoring the clarity of this same exact sentence indicating that "the RC time constant in the body link or recessed region 20 from a respective channel to the substrate contact 39"(emphasis added) is the concern.

In this last regard, the FR points to no teaching or suggestion in Chen, or any other reference, that indicates that even though the Chen statement is clear that the "C" of concern is that "in the body link or recessed region," the statement can be reasonably interpreted to actually say that it is the "capacitance of the MOS transistor"(as indicated at the top of page 3 of the FR) that is the concern. Rather than present concrete evidence as to why this clear statement would be interpreted to say that which it does not expressly state and which is contradictory to the express words of the statement, the examiner substitutes her subjective view that because other sources for capacitance are not apparent, the capacitance would be assumed to be a capacitance of the MOS transistor.

However, the question is not what the examiner subjectively believes to be apparent, it is what the reference itself states and reasonably suggests. In this regard, it is the burden of

the PTO to demonstrate a *prima facie* case of obviousness which means the PTO must show that the relied upon references teach all of the limitations of the claims without resort to speculation to fill gaps missing from reference teachings. Note the following from In re Warner, 154 USPQ 173, 178 (CCPA 1967):

> A rejection based on section 103 clearly must rest on a factual basis, and these facts must be interpreted without hindsight reconstruction of the invention from the prior art. In making this evaluation, all facts must be considered. The Patent Office has the initial duty of supplying the factual basis for its rejection. It may not, because it may doubt that the invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis. To the extent the Patent Office rulings are so supported, there is no basis for resolving doubts against their correctness. Likewise, we may not resolve doubts in favor of the Patent Office determination when there are deficiencies in the record as to the necessary factual bases supporting its legal conclusion of obviousness. [Emphasis added.]

Instead of pointing to a reasonable basis to interpret the statement that "the RC time constant in the body link or recessed region 20" as suggesting that "C" is actually the claimed gate capacitance, the FR resorts to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis by asserting that "MOS transistor" capacitance is the only source of capacitance in the Chen device. This assertion is first clearly mistaken because it ignores that the completed device of Chen will have wiring to the source, drain and gate of the transistors of the nature illustrated by FIG. 4, where such wiring has separate spacing capacitance as taught by Agari.

The FR is further mistaken in ignoring the limitation of concern in Claim 1 (and Claim 2, for that matter) requires "C" to be gate capacitance and not simply some form of stray capacitance or junction parasitic capacitance like the capacitances noted at col. 1, lines 20-22, or col. 5, lines 9-11, which is the parasitic capacitance under drain 28 and source 30 junctions of Chen. Moreover, Chen describes (in col. 3, lines 56-60) a doping concentration

of the recessed region 20 and the depletion width between the source and/or drain region and the recessed region 20. This further description clearly concerns the junction capacitance between the source and/or drain region and the recessed region 20 noted as to col. 5, lines 9-11, and it is well known that a capacitance value of such a junction capacitance is highly influenced by the doping concentration of the recessed region 20.

Furthermore, the response filed March 20, 2001, noted the following:

> In addition to lacking any evidence that the artisan would have some reason to consider the product of the resistance value R of a fixed potential transmission path extending from a body contact to a body region of the nature claimed and the capacitance value C of a gate of an MOS transistor formed on an oxide film over the body region to be important to control, the Action further lacks any evidence that the artisan would have a prior art based reason to believe that this RC product having an R value and a C value from different elements is somehow a measure of how quickly the signal decays as stated at the top of page 3 of the Action. Similarly lacking is some prior art based reason to believe that this particular RC product having an R value determined by an interior body region and a C value related to a gate electrode over an oxide layer of transistor should be minimized as to a clock signal period so as to produce some desired result. As noted by In re Sporck, 133 USPQ 360, 364 (CCPA 1962):
>
> > Obviousness is a legal conclusion which we ware required to draw from facts appearing in the record or of which judicial notice may be taken. Thus before we can conclude that any disclosed invention is 'obvious' under the conditions specified in 35 U.S.C. §103, we must evaluate facts from which to determine (1) what was shown in the prior art at the time the invention was made, and (2) the knowledge which a person of ordinary skill in the art possessed at the time the invention was made. Here, neither the record nor the facts of which we are able to take judicial notice supplies the factual data necessary to support the legal conclusion of obviousness of the invention at the time it was made. We are unwilling to substitute speculation and hindsight appraisal of the prior art for such factual data.

Thus, it is clear that the examiner improperly attempts to suggest that because Chen does not explain how the "C" portion of the referenced RC time constant arises because of doping in recessed region 20, she can substitute a speculative assumption that some form of

MOS transistor capacitance is really being referenced. Taking this speculative assumption one step further, gate capacitance is then, apparently, arbitrarily selected from known forms of transistor capacitance because this is what Claims 1 and 2 require and not because of any teaching or suggestion in any relied upon reference. The examiner, thus, does not reasonably attempt to supply a concrete factual basis for her rejection. Instead, she improperly substitutes speculation, unfounded assumptions, and hindsight reconstruction in clear violation of the above noted case law and the even more recent requirement for concrete evidence set forth by the PTO reviewing court in In re Zurko, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001) as follows:

> With respect to core factual findings in a determination of patentability, however, the Board cannot simply reach conclusions based on its own understanding or experience — or on its assessment of what would be basic knowledge or common sense. Rather, the Board must point to some concrete evidence in the record in support of these findings. [Emphasis added, foot note omitted.]

Just as the Board cannot substitute conclusions based upon its own understanding or experience for concrete evidence in the record, neither can the examiner.

Thus, it is believed to be clear that if the artisan where to reasonably follow the actual teachings of Agari and Chen to design the device of Iwamatsu, that artisan would merely use a step as to determining an optimum wiring line width and spacing to result in minimizing RC delay as to the wiring lines shown in the upper portion of Fig. 1 of Iwamatsu as taught by Agari and a separate doping step to dope body links between body contacts and MOS transistor channels so that these body links themselves would have a body link RC time constant as short as or less than 1 nsec. This is not the method set forth by either Claim 1 or the result of this method set forth by Claim 3.

Consequently, the rejection of Claims 1 and 3 should be reversed for the reasons noted above.

B. Claims 2 and 4

With specific regard to Claim 2 and 4, the discussion starting at the bottom of page 5 and continuing through the top of page 8 of the response filed March 20, 2001, is again believed to be relevant and is repeated here for the Board's convenience as follows:

> Turning to Claim 2, it is again noted that this claim is similar to Claim 1 as to the method of designing that is recited and the semiconductor device to be designed. The differences relate to the requirements of Claim 2 that relate to a signal propagation delay time being provided instead of the Claim 1 operating frequency and the determining of the layout pattern being based on this signal propagation delay time instead of the Claim 1 operating frequency. In this regard, Claim 2 requires the layout pattern to be determined so that (R·C) / td <1 with the definitions of R and C being the same for Claim 2 as for Claim 1 and "td" being the signal propagation delay time of the MOS transistor which must be less than or equal to 50 ps.
>
> Once again relative to Claim 2, it is believed to be clear that if the artisan where to reasonably use the teachings of Agari and Chen to design the device of Iwamatsu, he would merely add a step as to determining an optimum wiring line width and spacing to result in minimizing RC delay as to the wiring lines shown in the upper portion of Fig. 1 of Iwamatsu as taught by Agari and a separate doping step to dope body links between body contacts and MOS transistors so that these body links themselves have a body link RC time constant as short as or less than 1 nsec. This is not the method set forth by Claim 2.
>
> Similarly, with respect to independent Claim 2, the teachings of Agari cannot be based upon extracting terms out of context and assigning meanings thereto that are not consistent with the meanings clearly used by Agari. See again the Wesslau decision discussed above. The rejection of Claim 2 is also traversed as relying upon an improper interpretation of the language "wiring part" used by Agari just as the rejection of Claim 1 was.
>
> Moreover, and as noted above, even if Agari is assumed to somehow teach minimizing the RC time constant of a body contact, the body contact of Chen is just that, not any of the doped body links disclosed to be between body contacts and MOS transistors also taught by Chen. What Claim 2 requires, on the other hand, is the use of a layout pattern to form an MOS transistor on an SOI layer that will satisfy the conditional expression (R·C) / td > 1 where C = the gate capacitance of said MOS transistor, R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region, and td = signal propagation delay time required for the MOS transistor, with td being less than or equal to 50 ps. None of Iwamatsu, Agari, or Chen teach any reason at all to consider multiplying the resistance value R of a fixed potential transmission path

extending from a body contact to a body region of the nature claimed by the capacitance value C of a gate of an MOS transistor formed on an oxide film over the body region and multiplying the result by a signal propagation delay time td required for the MOS transistor, with td being less than or equal to 50 ps and insuring that the final result is less than one.

Clearly, the resistance "R" of concern in Claim 2 is again that of a "fixed potential transmission path" extending from a body contact to a body region as discussed above and not the resistance of the wiring line of concern to Agari. In addition none of Iwamatsu, Agari, or Chen teach any reason to use the capacitance "C" of the MOS transistor gate electrode along with this value R of an internal transmission path to form an RC product, much less one that meets the Claim 2 requirement that (R·C) / td <1 with td being less than or equal to 50 ps. Once again, valid rejections can only be made if they are based upon established facts as to the prior art. The rejection of Claim 2 is also traversed because speculation and hindsight based upon applicants' disclosure have again been used as a substitute for facts not of record.

Consequently, the rejection of Claims 2 and 4 should be reversed for the reasons noted above.

C. Claims 5 and 18

Claims 5 and 18 are specific to a semiconductor device having a particular resistance for the fixed potential transmission path primarily determined by body region 14 resistance defined in part by the thickness of the SOI layer times the length of the fixed potential transmission path along the gate length of the gate electrode. The various Office Action have not set forth any attempt at a *prima facie* case of obviousness that addresses these limitations. Without such a *prima facie* case of obviousness, reversal is mandatory. See In re Fine, 5 USPQ2d 1596, 1598-99 (Fed. Cir. 1988).

Consequently, the rejection of Claims 5 and 18 should be reversed for the reasons noted above.

CONCLUSION

The rejection as applied to Claims 1-5 and 18 should be reversed for the above-noted reasons.

Respectfully submitted,

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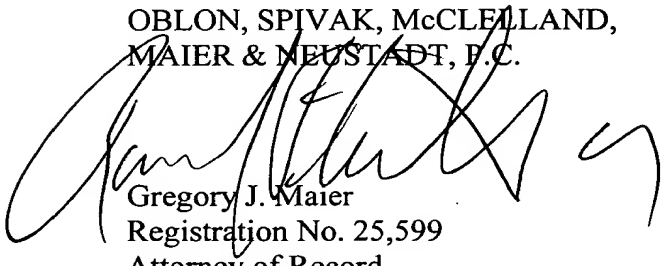

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APPENDIX

1. A method of designing a semiconductor device including a MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer, said MOS transistor being operated based on a predetermined clock,

said MOS transistor comprising:

a first semiconductor region of a first conductivity type and selectively formed in said SOI layer;

a second semiconductor region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region;

a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions;

a gate electrode formed on a gate oxide film formed on said body region; and

at least one body contact electrically connected to said body portion and receiving a fixed potential,

said method comprising the steps of:

(a) providing an operating frequency of said predetermined clock; and

(b) determining a layout pattern of said MOS transistor based on the operating frequency of said predetermined clock,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression

$$R \cdot C \cdot f < 1$$

where

C = the gate capacitance said MOS transistor,

R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region,

f = the operating frequency of said predetermined clock, and

$f \geqq 500$ MHZ.

2. A method of designing a semiconductor device including a MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer,

said MOS transistor comprising:

a first semiconductor region of a first conductivity type and selectively formed in said SOI layer;

a second semiconductor region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region;

a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions;

a gate electrode formed on a gate oxide film formed on said body region, said gate electrode being electrically connected to said body portion; and

at least one body contact electrically connected to said body portion and receiving a fixed potential,

said method comprising the steps of:

(a) providing a signal propagation delay time required for said MOS transistor; and

(b) determining a layout pattern of said MOS transistor based on said signal propagation delay time,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression

$(R \cdot C)/td < 1$

where

C = the gate capacitance of said MOS transistor,

R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region,

td = signal propagation delay time (s) required for said MOS transistor, and

$td \leqq 50$ ps.

3. A semiconductor device designed by the method as recited in claim 1.

4. A semiconductor device designed by the method as recited in claim 2.

5. The semiconductor device according to claim 3,

wherein said resistance R of said fixed potential transmission path is determined by

$R = (\rho \cdot W)/(L \cdot t_{SOI})$

where

W = the length of said fixed potential transmission path in said body region along the gate width of said gate electrode,

L = the length of said fixed potential transmission path in said body region along the gate length of said gate electrode,

t_{SOI} = the thickness of said SOI layer, and

ρ = the resistivity of said body region.

18. The semiconductor device according to claim 4,

wherein said resistance R of said fixed potential transmission path is a determined by

$R = (\rho \cdot W)/(L\text{-}t_{SOI})$ where

W = the length of said fixed potential transmission path in said body region along the gate width of said gate electrode,

L = the length of said fixed potential transmission path in said body region along the gate length of said gate electrode,

t_{SOI} = the thickness of said SOI layer, and

ρ = the resistivity of said body region.